COMPOUND FIELD EFFECT TRANSISTOR WITH MULTI-FEED GATE AND SERPENTINE INTERCONNECT

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This continuation application claims the priority benefit of U.S. patent application number 13/205,433, filed Aug. 8, 2011, and titled "LOW INTERCONNECT RESISTANCE INTEGRATED SWITCHES," which claims the priority benefit of U.S. provisional application No. 61/372,513, filed Aug. 10, 2010, and titled "Field Effect Transistor and Method of Making Same." The above referenced applications are hereby incorporated by reference in their entirety.

TECHNICAL FIELD

[0002] The present invention relates to semiconductors devices, and more particularly to compound semiconductor Field Effect Transistor switches and power FETs.

BACKGROUND

[0003] A common type of Field Effect Transistors (FET) is a Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), which may be fabricated using silicon. A FET may also be fabricated using germanium or a compound semiconductor such as gallium arsenide (GaAs) or gallium nitride (GaN). FET devices fabricated from compound semiconductors such as GaAs make very good switches and signal amplification devices for rf and microwave applications. Among these devices are switches and large-signal (or power) amplifier circuits. Some advantages of compound semiconductor FET switches over silicon MOSFET switches include high blocking (off-state) resistance, low on-state resistance (RDs (on)), fast switching speed, high current density, low temperature coefficient, high junction temperature and, for GaN devices, high breakdown voltage. Unfortunately, compound semiconductor FET switches and power FETs are also more expensive to manufacture than silicon MOSFETs due to the larger size of the FETs necessary to handle power, smaller wafers and higher fabrication expenses. Merely decreasing the size of compound semiconductors by scaling down the device may not decrease costs.

SUMMARY

[0004] Device cost of a compound semiconductor switching or power FET is driven by two factors, namely size and yield. The present invention addresses both. Reducing the size while maintaining current handling capabilities is accomplished by distributing portions of the current handled by the device in parallel to sections the source and drain fingers to maintain a low current density and eliminate outboard bonding pads. Increasing yield is accomplished by applying the gate signal to both ends of the gate fingers, which eliminates a major source of device failure, i.e., a break in any single one of the many gate fingers. The current to be handled by the FET may be divided among a set of electrodes arrayed along the width of the source or drain fingers. The electrodes may be oriented to cross the fingers along the length of the array of source and drain fingers. The portion of the current distributed to each source electrode may be coupled to a section of each source finger crossed by the source electrode. Similarly, the portion of the current distributed to each drain electrode may be applied to a section of each drain finger crossed by the drain electrode. The current may be conducted from the source and drain electrodes to the source and drain fingers, respectively, through vias disposed along the surface of the fingers. Heat developed in the source, drain, and gate fingers may be conducted through the vias to the electrodes and out of the device.

[0005] Various aspects of a means for switching current using a Field Effect Transistor comprises a means for segmenting source current and a means for distributing segments of the segmented source current to sections of a source finger disposed on a surface of a gallium arsenide semiconductor. The FET means further includes a means for segmenting drain current and a means for distributing segments of the segmented drain current to sections of a drain finger disposed on the surface of the gallium arsenide, and a means for coupling a gate signal to two ends of a gate finger disposed between the source element and the gate element.

[0006] Various embodiments of a Field Effect Transistor device comprises a compound semiconductor substrate, a plurality of source fingers disposed on a surface of the substrate and a plurality drain fingers disposed on the surface of the substrate and alternating with the source fingers. The FET device further comprises a plurality of gates disposed between adjacent source fingers and drain fingers. The FET device also includes a plurality of first gate pads each configured to couple a gate signal to a first end of at least one of the gate fingers and a plurality of second gate pads each configured to couple the gate signal to a second end of at least one of the gate fingers. A dielectric layer may be disposed on the source fingers, drain fingers and gate fingers. A plurality of source electrodes may be disposed on the dielectric layer along a width of the source fingers and oriented to cross the plurality of source fingers, each electrode electrically coupled through at least one via in the dielectric layer to a section of each of the source fingers. A plurality of drain electrodes may be disposed on the dielectric layer along a width of the drain fingers and oriented to cross the plurality of drain fingers, each electrode electrically coupled through at least one via in the dielectric layer to a section of each of the drain fingers.

[0007] Various aspects of a method for switching current using a Field Effect Transistor comprises partitioning source current into a plurality of source current segments for distribution along a width of a source element of the Field Effect Transistor and distributing the plurality of source current segments to sections of the source element through a plurality of source electrodes, each electrode in electrical contact with at least one of a plurality of vias distributed along a surface of the source element. The method further comprises partitioning drain current into a plurality of drain current segments for distribution along a width of a drain element of the Field Effect Transistor, the drain element disposed adjacent the source element and distributing the plurality of drain current segments to sections of the drain element through a plurality of drain electrodes, each electrode in electrical contact with at least one of a plurality of vias distributed along a surface of the drain element. The method also includes coupling a gate signal to a first and second end of a gate finger disposed between the adjacent source and gate elements, and switching current between the source element and the drain element using the gate signal coupled to the ends of the gate finger.

[0008] In various embodiments, the Field Effect Transistor device comprises a compound semiconductor layer, a first and second source finger disposed on a surface of the compound semiconductor layer and a first and second drain finger